



2823  
11/03/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daniel Xu

Serial No.: 09/975,163

Filed: October 11, 2001

For: Forming Tapered Lower Electrode  
Phase-Change Memories

§ Group Art Unit: 2823  
§  
§  
§ Examiner: Brook Kebede  
§  
§  
§ Atty. Dkt. No.: ITO.0508US (P12501)  
§

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

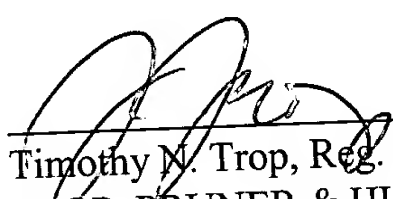
Applicant submits the references listed on the attached form PTO 1449 together with any required copies of such references.

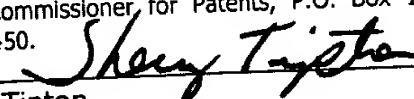
This statement is being filed before the receipt of a first Office action on the merits.

Please apply any charges or credits to Deposit Account 20-1504 (ITO.0508US).

Respectfully submitted,

Date: 10/30/03

  
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Date of Deposit: 10-30-03  
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.  
  
Sherry Tipton

|   |    |   |      |                          |       |          |                               |
|---|----|---|------|--------------------------|-------|----------|-------------------------------|
| <b>INFORMATION DISCLOSURE CITATION</b><br>(Use several sheets if necessary)   |    | ATTY DOCKET NO.<br>ITO.0508US (P12501)  |      | SERIAL NO.<br>09/975,163 |       |          |                               |
|   |    | APPLICANT(S):<br>DANIEL XU  |      |                          |       |          |                               |
|   |    | FILING DATE:<br>October 11, 2001  |      | GROUP ART UNIT:<br>2823  |       |          |                               |
| <b>U.S. PATENT DOCUMENTS</b>  |    |   |      |                          |       |          |                               |
| *EXAMINER<br>INITIAL  | A. | DOCUMENT NUMBER   | DATE | NAME                     | CLASS | SUBCLASS | FILING DATE<br>IF APPROPRIATE |
|   | B. |   |      |                          |       |          |                               |
|   | C. |   |      |                          |       |          |                               |
|   | D. |   |      |                          |       |          |                               |
| <b>FOREIGN PATENT DOCUMENTS</b>   |    |   |      |                          |       |          |                               |
|   |    | DOCUMENT NUMBER   | DATE | COUNTRY                  | CLASS | SUBCLASS | TRANSLATION<br>YES NO         |
|   | E. |   |      |                          |       |          |                               |
|   | F. |   |      |                          |       |          |                               |
|   | G. |   |      |                          |       |          |                               |
|   | H. |   |      |                          |       |          |                               |
| <b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.) |    |   |      |                          |       |          |                               |
|   | I. | Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Jeong, U.I., Jeong, H.S. and Kim, Kinam, "Completely CMOS-Compatible Phase-Change Nonvolatile RAM Using NMOS Cell Transistors," presented at 2003 19 <sup>th</sup> IEEE Non-Volatile Semiconductor Memory Workshop, Monterey, California, February 26-20, 2003 |      |                          |       |          |                               |
|   | J. | Ha, Y.H., Yi, J.H., Horii, H., Park, J.H., Joo, S.H., Park, S.O., Chung, U-In and Moon, J.T., "An Edge Contact Type Cell for Phase Change RAM Featuring Very Low Power Consumption," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003  |      |                          |       |          |                               |
|   | K. | Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Oh, J.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Chung, U.I., Jeong, H.S. and Kim, Kinam, "Full Integration and Reliability Evaluation of Phase-change RAM Based on 0.24 mm-CMOS Technologies," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003                   |      |                          |       |          |                               |
|   | L. | Horii, H., Yi, J.H., Park, J.H., Ha, Y.H., Baek, I.G., Park, S.O., Hwang, Y.N., Lee, S.H., Kim, Y.T., Lee, K.H., Chung, U-In and Moon, J.T., "A Novel Cell Technology Using N-doped GeSbTe Films for Phase Change RAM," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003   |      |                          |       |          |                               |
|   | M. |   |      |                          |       |          |                               |
|   | N. |   |      |                          |       |          |                               |
|   | O. |   |      |                          |       |          |                               |
| EXAMINER  |    |   |      | DATE CONSIDERED          |       |          |                               |

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.